

M5003 Series

9x16 mm FR-4, 3.3 Volt, CMOS/TTL/PECL/LVDS, HPVCXO



- Ideal for applications requiring long term (20 year) all-inclusive stability

Ordering Information

00.0000
MHz

M5003 2 0 R 1 P K -R

Product Series _____

Temperature Range _____

1: 0°C to +70°C 2: -40°C to +85°C
6: -20°C to +70°C 7: 0°C to +85°C

Stability _____

0: Nominal per APR selection

Output Type _____

R: Complementary tri-state (PECL/LVDS)
T: Tri-state (CMOS)

Absolute Pull Range (APR) _____

1: ±25 ppm
2: ±15 ppm

Symmetry/Logic Compatibility _____

D: 45/55% CMOS/TTL L: 45/55% LVDS
P: 45/55% PECL

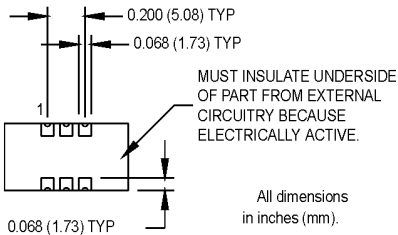
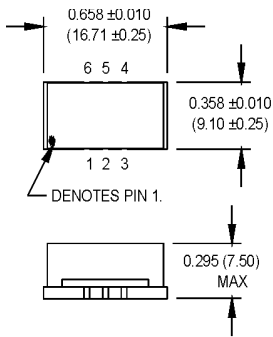
Package/Lead Configurations _____

K: FR-4, 6-Pad

RoHS Compliance _____

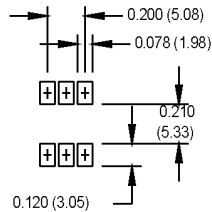
Blank: non-RoHS compliant part
-R: RoHS compliant part

Frequency (customer specified) _____



All dimensions in inches (mm).

SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Tristate
3	Ground
4	Output 1
5	N/C or Output 2
6	+Vdd

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	1 19.44		160 800	MHz MHz	CMOS/TTL PECL/LVDS	
Operating Temperature	T _A	(See Ordering Information)					
Storage Temperature	T _s	-55		+105	°C		
Frequency Stability	ΔF/F	(See Ordering Information)					See Note 1
Aging							
1st Year				1.5	ppm		
Thereafter (per year)				0.5	ppm		
Pullability/APR		(See Ordering Information)					Over Control Voltage
Control Voltage	V _c	0.3	1.65	3.0	V		
Tuning Range				25	ppm/V		
Modulation Bandwidth	f _m	10			kHz		
Input Impedance	Z _{in}	50K			Ohms		
Input Voltage	V _{cc} /V _{dd}	3.15	3.3	3.45	V		
Input Current	I _{cc} /I _{dd}	5 50 5		50 120 75	mA mA mA	CMOS/TTL PECL LVDS	
Output Type							CMOS/TTL/PECL/LVDS
Load		2 TTL or 15 pF Max. 50 Ohms to V _{cc} -2 Volts 100 Ohm differential load					CMOS/TTL PECL LVDS
Symmetry (Duty Cycle)		(See Ordering Information)					
Output Skew				50	ps	PECL	
Differential Voltage		250	375	500	mV	LVDS	
Logic "1" Level	V _{oh}	2.5 2.2 1.375		2.4	V V V	CMOS/TTL PECL LVDS	
Logic "0" Level	V _{ol}	1.4		0.5 1.7 1.125	V V V	CMOS/TTL PECL LVDS	
Rise/Fall Time	T _r /T _f	2.0 0.25		10 3.0	ns ns	CMOS/TTL PECL/LVDS	
Tristate Function		Input Logic "1": output active Input Logic "0": output disables					Opposite tristate logic Available upon request
Start up Time		10					ms
Phase Noise (Typical)		10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier
@ 19.44 MHz		-60	-90	-120	-135	-148	dBc/Hz
@ 155.52 MHz		-60	-90	-110	-120	-120	dBc/Hz
@ 622.08 MHz		-60	-90	-100	-105	-105	dBc/Hz

1. Stability includes initial tolerance, deviation over temperature, supply and load variation, and aging for 20 years @ 25°C.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.

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